IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:

Kraig R. WHITE

Docket No.: FIS920010178US1

Serial No.: 10/066,497

Group Art Unit: 2133

Filed: February 1, 2002

Examiner: TORRES, Joseph D.

For: **CHECK BIT FREE ERROR CORRECTION FOR SLEEP MODE DATA RETENTION**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

DECLARATION UNDER 37 C.F.R. 1.131

Sir:

I, Kraig R. White, do hereby declare:

1. I am the inventor of the subject matter disclosed and recited in independent claims 1, 10, and 15 of the above-identified application.

2. I completed the invention of claims 1, 10, and 15 (and those claims dependent thereon) in the United States **before August 8, 2001**, as evidenced below.

CONCEPTION

3. Before August 8, 2001, I conceived of a memory system having a reduced refresh rate in a sleep mode as disclosed and recited in independent claim 1 of the application. Also before August 8, 2001, I further conceived a method for reducing the refresh rate of a memory in sleep mode as disclosed and recited in independent claims 10 and 15 of the application. Such conception is evidenced by invention disclosure documentation attached hereto as Exhibit A.

The invention disclosure documentation attached hereto is a photocopy of and is identical to the originals, except that all pertinent dates have been removed therefrom.

4. All pertinent dates removed from the invention disclosure documentation attached hereto are before August 8, 2001.

5. As evidenced by Exhibit A, the memory system having a reduced refresh rate includes:

a. a dynamic memory;

b. an error correction code (ECC) memory allocation circuit for identifying non-critical bit addresses in said dynamic memory and allocating said addresses as ECC addresses when entering from an active mode to sleep mode;

c. an ECC encoder for encoding critical bits with error correction codes, said error correction codes being stored in said ECC addresses;

d. a refresh execution circuit for reducing a refresh rate in said sleep mode and increasing said refresh rate in said active mode; and

e. an ECC decoder for decoding said critical bits encoded with said error correction codes when reentering said active mode.

6. In further embodiments, as evidenced by Exhibit A, the method for reducing the refresh rate of a memory in sleep mode also includes, for example:

a. switching from an active mode to a sleep mode;

b. identifying non-critical bit addresses;

c. encoding critical bits with an error correction code (ECC);

d. storing ECC codes at said non-critical bit addresses;

e. reducing a refresh rate for said memory;

f. performing error correction on said critical bits using said ECC codes when reentering active mode; and

g. discarding said ECC bits.

7. The benefits and features of the memory system having a reduced refresh rate in a sleep mode, as well as the method for reducing the refresh rate of a memory in sleep mode are shown and described in the invention disclosure.

8. These features and others are exemplified in the figures in at least the invention disclosure documentation, all of which is a complete and permanent idea of the complete and operable invention.

DUE DILIGENCE

9. Prior to August 8, 2001, I worked diligently on the invention as recited in the claims of the above-identified application until such application was completed and filed on February 1, 2002.

10. From a date prior to August 8, 2001, I worked diligently to provide information to IBM in-house counsel in order to begin the preparation of a patent application for filing in the U.S. Patent Office. As a result, I completed the attached invention disclosure and communicated its pertinent information relating to the inventive concept to IBM in-house counsel before August 8, 2001.

11. Prior to the filing of the above-identified application in the U.S. Patent Office, I communicated with patent counsel at McGuireWoods LLP, to prepare such patent application based on the submitted invention disclosure. I further worked diligently on the preparation of the patent application with patent counsel at McGuireWoods until a final draft patent application was completed to my satisfaction. Additionally, I participated in reviewing and finalizing the application for the present invention prior to the filing of the above-identified application. For example, communications took place on at least May 8, 2001, August 27, 2001, October 25, 2001, and up to and including correspondences dated January 12, 2002.

12. A final draft of the application was forwarded to me by IBM in-house attorney, Daryl K. Neff, who received the final draft from then McGuireWoods' attorney Kevin Reif in a letter dated January 12, 2002. As evidenced herein, I worked diligently at all times to finalize the application for filing in the U.S. Patent and Trademark Office from prior to August 8, 2001 to the time the finalized application was filed on February 1, 2002.

13. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that the statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon

Kraig R. White

Kraig R. White

8/23/04

Date

EXHIBIT A

Disclosure BUR8

Prepared for and/or by an IBM Attorney - IBM Confidential

Created By: Kraig White **Created On:**
Last Modified By: Cynthia Hill **Last Modified On:**

Required fields are marked with the asterisk (*) and must be filled in to complete the form.

***Title of disclosure (in English)**

Check bit free Error Correction for "sleep mode" data retention

Summary

Status	Awaiting Search
Original Location	BUR
Processing Location	FIS
Functional Area	EBJ Embedded Memory Circuits & Architectures - EDRAM, GRAM ... 140V
Attorney/Patent Professional	Steven Capella/Fishkill/IBM
IDT Team	Michael Clinton/Burlington/IBM
Submitted Date	
Owning Division	MD
Incentive Program	
Lab	Carswell
Technology Code	140V
PVT Score	38

Inventors with Lotus Notes IDs

Inventors: Kraig White/Burlington/IBM

Inventor Name	Inventor Serial	Div/Dept	Inventor Phone	Manager Name
> White, K.R. (Kraig)	696363	29/DEFV	N/A	Kilmer, C.A. (Art)

> denotes primary contact

Inventors without Lotus Notes IDs

IDT Selection

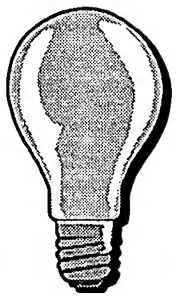
Select Functional Area

IDT Team:	Attorney/Patent Professional:
Michael Clinton/Burlington/IBM	Steven Capella/Fishkill/IBM

Response Due to IP&L :

Sleep Mode ECC

Check Bit free ECC



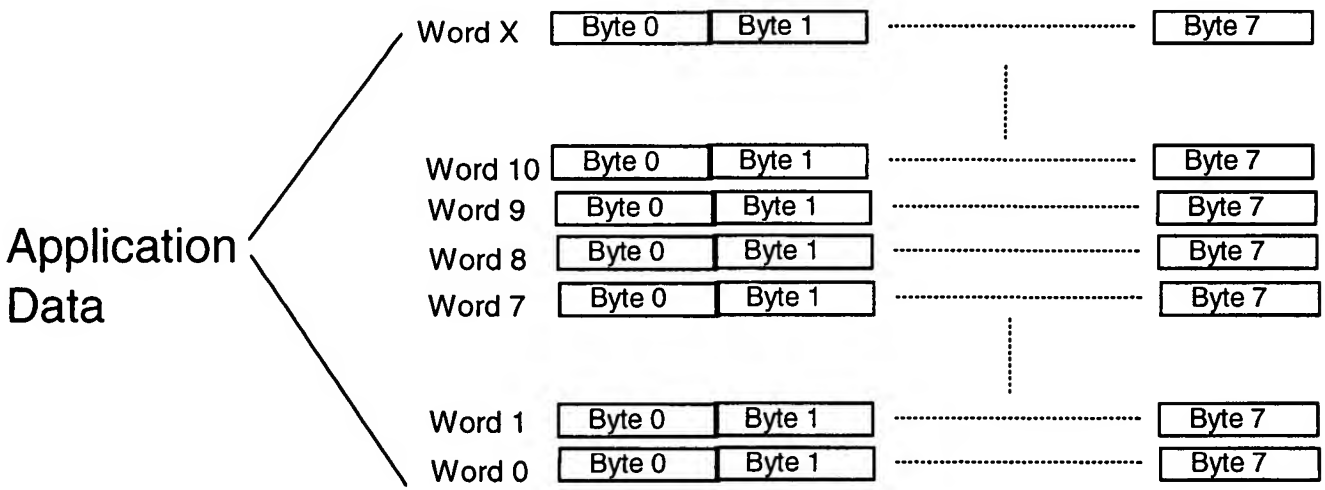
Concept:

- During normal operation, all DRAM bits are available for end application utilization
- Prior to entering Sleep Mode, non critical bits are identified and made available for storing Error Correction Code bits
- During SM, end application critical bits and ECC bits are maintained via refresh cycles
- Upon exiting SM, ECC is used to correct any retention time fails that occured during Sleep; ECC bits are discarded and the total DRAM becomes available for end application utilization

Projected benefit:

- Mavrick retention time fails are tolerated by the application thereby facilitating
  - ✓ Single temperature retention time testing (e.g. 80ms prefuse Wafer Test at 100◦C)
  - ✓ Longer SM retention time (e.g. 80ms at 85◦C ambient; >600ms at 40◦C??)
- SM ECC implemented without extra DRAM bits being required and the design of an ECC architected macro (e.g. x288 bit data interface)

Example: Normal Operation



Sleep Mode

Application Data